Confirmation No. 4378

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	HUETING *et al.*	Examiner:	Hsieh, H.
Serial No.:	10/580,625	Group Art Unit:	2811
Filed:	May 24, 2006	Docket No.:	GB030212US (NXPS.403PA)
Title:	TRENCH INSULATED GATE FIELD EFFECT TRANSISTOR HAVING A FIELD PLATE ELECTRODE		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed November 19, 2010 and in response to the rejections of claims 1-21 as set forth in the Final Office Action dated July 22, 2010.

Please charge Deposit Account number 50-4019 (GB030212US) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-4019 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-21 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

An amendment was filed on September 22, 2010 in response to the Final Office Action dated July 22, 2010. The Advisory Action dated October 15, 2010 indicates that the amendment was entered.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1: an insulated gate field effect transistor, comprising: a semiconductor body (*see, e.g.*, Fig. 1, element 2; p. 6:8-10) having opposed first and second major surfaces (*see, e.g.*, Fig. 1, elements 4, 6; p. 6:8-10); a source region of a first conductivity type at the first major surface (*see, e.g.*, Fig. 1, element 14; p. 6:10-16); a body region of a second conductivity type opposite to the first conductivity type under the source region (*see, e.g.*, Fig. 1, element 12; p. 6:10-16); a drift region of the first conductivity type under the body region (*see, e.g.*, Fig. 1, element 19; p. 6:10-16); a drain region of the first conductivity type under the drift region (*see, e.g.*, Fig. 1, element 8; p. 6:10-16), so that the source, body, drift and drain regions extend in that order from the first major surface towards the second major surface (*see, e.g.*, Fig. 1; p. 6:8-20); and insulated trenches extending from the first major surface towards the second major surface past the source region and the body region into the drift region (*see, e.g.*, Fig. 1, element 20; p. 6:16-20), each insulated trench having sidewalls (*see, e.g.*, Fig. 1, element 22; p. 6: 16-20), and including insulator on the sidewalls (*see, e.g.*, p. 6: 20-32), at least one conductive gate electrode (*see, e.g.*, Fig. 2, element 32; p. 6: 20-32) adjacent to the body region separated from the body region by a gate insulator, and at least one conductive field plate electrode (*see, e.g.*, Figs. 1-3, element 34; p. 6: 20-32) adjacent to the drift region separated from the drift region by a field plate insulator (*see, e.g.*, Figs. 1-3, element 30; p. 6: 20-32), and a gate-field plate insulator (*see, e.g.*, Figs. 1-3, element 28; p. 6: 20-32) separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being at least as thick as the field plate insulator (*see, e.g.*, p. 6: 20-32), wherein the source regions and the insulated trenches define a pattern of cells across the first major surface (*see, e.g.*, Figs. 1-3, element 28; p. 6: 8-32); and a doping concentration in the drift region increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region the doping concentration in the drift region being at least 50 times greater adjacent to the drain region than adjacent to the body region (*see, e.g.*, pp. 3:6-10; 7:16-9:23).

Commensurate with independent claim 15: an insulated gate field effect transistor, comprising: a semiconductor body (*see, e.g.*, Fig. 1, element 2; p. 6:8-10) having opposed first and second major surfaces (*see, e.g.*, Fig. 1, elements 4, 6; p. 6:8-10); a source region of a first conductivity type at the first major surface (*see, e.g.*, Fig. 1, element 14; p. 6:10-16); a

body region of a second conductivity type opposite to the first conductivity type under the source region (*see, e.g.*, Fig. 1, element 12; p. 6:10-16); a drift region of the first conductivity type under the body region (*see, e.g.*, Fig. 1, element 19; p. 6:10-16); a drain region of the first conductivity type under the drift region (*see, e.g.*, Fig. 1, element 8; p. 6:10-16), so that the source, body, drift and drain regions extend in that order from the first major surface towards the second major surface (*see, e.g.*, Fig. 1; p. 6:8-20); and insulated trenches extending from the first major surface towards the second major surface past the source region and the body region into the drift region (*see, e.g.*, Fig. 1, element 20; p. 6:16-20), each insulated trench having sidewalls(*see, e.g.*, Fig. 1, element 22; p. 6: 16-20), and including insulator on the sidewalls (*see, e.g.*, p. 6: 20-32), at least one conductive gate electrode (*see, e.g.*, Fig. 2, element 32; p. 6: 20-32) adjacent to the body region separated from the body region by a gate insulator, and at least one conductive field plate electrode (*see, e.g.*, Figs. 1-3, element 34; p. 6: 20-32) adjacent to the drift region separated from the drift region by a field plate insulator (*see, e.g.*, Figs. 1-3, element 30; p. 6: 20-32), and a gate-field plate insulator (*see, e.g.*, Figs. 1-3, element 28; p. 6: 20-32) separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being thicker than the field plate insulator (*see, e.g.*, p. 6: 20-32), wherein the source regions and the insulated trenches define a pattern of cells across the first major surface (*see, e.g.*, Figs. 1-3, element 28; p. 6: 8-32); and wherein the drift region has a graded doping concentration that increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region, the doping concentration in the part of the drift region adjacent to the drain region being at least 50 times greater than the doping concentration in the part of the drift region adjacent to the body region (*see, e.g.*, pp. 3:6-10; 7:16-9:23).

Commensurate with independent claim 19, an insulated gate field effect transistor, comprising: a semiconductor body (*see, e.g.*, Fig. 1, element 2; p. 6:8-10) having opposed first and second major surfaces (*see, e.g.*, Fig. 1, elements 4, 6; p. 6:8-10); a source region at the first major surface(*see, e.g.*, Fig. 1, element 14; p. 6:10-16), a body region under the source region (*see, e.g.*, Fig. 1, element 12; p. 6:10-16), a drift region (*see, e.g.*, Fig. 1, element 19; p. 6:10-16) under the body region, and a drain region under the drift region (*see, e.g.*, Fig. 1, element 8; p. 6:10-16), the drift region having a doping concentration that

increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region, the doping concentration in the drift region being at least 50 times greater adjacent to the drain region than adjacent to the body region (*see, e.g.*, pp. 3:6-10; 7:16-9:23); and a plurality of insulated trenches extending from the first major surface into the drift region (*see, e.g.*, Fig. 1, element 20; p. 6:16-20), each of the insulated trenches including at least one conductive gate electrode (*see, e.g.*, Fig. 2, element 32; p. 6: 20-32) adjacent to the body region and separated from the body region by a gate insulator, at least one conductive field plate electrode (*see, e.g.*, Figs. 1-3, element 34; p. 6: 20-32) adjacent to the drift region and separated from the drift region by a field plate insulator (*see, e.g.*, Figs. 1-3, element 30; p. 6: 20-32), and a gate-field plate insulator (*see, e.g.*, Figs. 1-3, element 28; p. 6: 20-32) separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being at least as thick as the field plate insulator (*see, e.g.*, p. 6: 20-32), wherein the source regions and the insulated trenches define a pattern of cells across the first major surface (*see, e.g.*, Figs. 1-3, element 28; p. 6: 8-32).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1, 4-7, 9-10,12-19 and 21 stand rejected under 35 U.S.C. § 103(a) over Omura (EP 1168455).

B. Claims 2 and 11 stand rejected under 35 U.S.C. § 103(a) over the '455 reference in view of Onda *et al.* ("SIC Integrated MOSFETs" Physica Status Solidi (A), Applied Research, Berlin, DE, vol.162, no. 1, 16 July 1997, pages 369-388).

C. Claims 3 and 20 stand rejected under 35 U.S.C. § 103(a) over the '455 reference in view of Miyano *et al.* (JP 403211885).

D. Claim 8 stands rejected under 35 U.S.C. § 103(a) over the '455 reference in view of Hshieh *et al.* (U.S. Patent Pub. 2001/0003367).

VII. Argument

It is not disputed that the cited references fail to teach express or implicit correspondence to all limitations of the claims. The missing limitations have been alleged to be obvious because they are subject to "routine experimentation" (Final Office Action, p. 6).

As discussed in more detail hereafter, the factual evidence in favor of the Examiner's position is virtually nonexistent and the evidence weighing in favor of patentability is significant and in some cases has been expressly (and improperly) excluded from the Examiner's consideration. The proper legal standard is "a preponderance of evidence" and requires the evidence to be more convincing than the evidence which is offered in opposition to it. The following discussion establishes that for each rejection the factual evidence is disproportionally in favor of patentability and that the rejections must be reversed.

It is noted that each of the rejections relies upon the same underlying assertion of correspondence/obviousness, which is based upon the primary '455 reference. None of the additionally-cited references and proposed modifications cures or is alleged to cure the issues raised in connection with the underlying assertions. To facilitate review efforts, the claims have been grouped accordingly.

A. The Rejections of Claims 1-21 are Improper for Lack of Correspondence and Lack of Evidentiary Support Regarding a Gate-Field Plate Insulator that is at Least as Thick as a Field Plate Insulator

Appellant's specification expressly states that that prior art "structures with field plates are known for use with high break down voltage of at least 50V and generally higher" (p. 3:20-21). Appellant's specification further explains the surprising finding that "field plate structures are also applicable to low voltage power MOS-FETs with breakdown voltages of 30V and below, even though the channel resistance forms the major contribution to resistance in such devices" (p. 3:21-24). Thus, Appellant's specification teaches a specific configuration of elements, which includes both the field plate insulator thickness and doping concentrations that are not believed to be taught by the relevant prior art. Further details of these and other such teachings are found in subsequent portions of the specification (*see, e.g.*, p. 8, *et seq.*)

The Examiner does not dispute that these surprising results were not known, and presents no evidence to rebut that these results were unexepcted. Rather than address these considerations, the Examiner concludes that limtiations useful for realizing these surprising results need not be addressed other than to conclude that experimentation renders them obvious. The Examiner fails to support this conclusion with realistic goals and

corresponding modifications, relying upon general conculsions that present an erroneous one-sided assessment of the relevant evidentiary factors.

For example, the central purpose of the primary '455 reference is a "power semiconductor switching element ... having a low ON resistance" (p. 2:3-4). "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." (M.P.E.P. 2143.01, citing *In re Ratti*, 270 F.2d 810 (CCPA 1959)). A review of the teachings of the primary '455 reference confirms that this is a primary goal (*see, e.g.*, p. 7:1-43 discussing many different manners to reduce ON resistance). Thus, attempts to modify the central teachings of the '455 reference (*i.e.*, to increase the ON resistance) are not sufficient for even a *prima facie* rejection. For example, it would be illogical for the skilled artisan to use the primary '455 reference's teachings, which are specially designed to produce a device with a low ON resistance, only to undertake open-ended experimentation toward a solution that would be expected to increase the ON resistance. If the skilled artisan's "desired device performance" was a transistor with higher ON resistance and lower breakdown voltage, as suggested by the Examiner, it seems illogical to allege that the skilled artisan would choose the teachings of the primary '455 reference as a basis to achieve this "desired device performance." Accordingly, the rejection should be reversed because it requires the skilled artisan to modify the teachings of the primary '455 reference in a manner that contradicts the central purpose taught by the primary '455 reference.

Moreover, a *prima facie* could not be presented with new arguments because the amount of evidence which overcomes the rejection would not be addressed. For example, the Examiner has not properly considered the claim limitations as a whole. The Examiner oversimplifies the obviousness analysis by focusing primarily upon the individual differences between the claim limitations and the teachings of the '455 reference. "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." (M.P.E.P. § 2141.02 (emphasis original), citing *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530 (Fed. Cir. 1983); *Schenck v. Nortron*

Corp., 713 F.2d 782 (Fed. Cir. 1983)). "(A)n obviousness finding was appropriate where the prior art contained detailed enabling methodology for practicing the claimed invention, a suggestion to modify the prior art to practice the claimed invention, and evidence suggesting that it would be successful." (internal citations omitted) *In re Kubin*, 561 F.3d 1351, 1360 (Fed. Cir. 2009). The Examiner's analysis focuses primarily upon on the specific differences of the claim limitations without providing factual evidence of detailed enabling methodology, suggestion to modify or evidence suggesting that the modification would be successful. Isolating such differences and then using hindsight reasoning to conclude the individual differences would have been obvious to experiment towards is the hallmark of improper hindsight reconstruction. For instance, the Examiner fails to consider that there are any number of potential variables that could be selected for experimentation and that each variable has large numbers of potential values. Moreover, the primary '455 reference fails to teach how interrelationships between these variables would be expected to function relative to the Examiner's proposed experimentations.

In this context, the Examiner has improperly asserted that the proposed modification would have been obvious to try based upon a hindsight selection of unspecified parameters, conjecture and experiments to be performed thereon. Rejections are improper when "what would have been 'obvious to try' would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result ... courts should not succumb to hindsight claims of obviousness." *In re Kubin*, 561 F.3d 1351, 1359 (Fed. Cir. 2009). *See also* M.P.E.P. § 2143(E), and *Gillette Co. v. S.C. Johnson & Son, Inc.*, 919 F.2d 720, 725 (Fed. Cir. 1990) ("we have consistently held that 'obvious to try' is not to be equated with obviousness."). The Examiner's routine experimentation is not at all routine or suggested for a varsity of reasons, as indicated both by the absence of evidence or explanation in support of Examiner's position and by the teaching-away evidence discussed below.

Further factual evidence of the improper nature of the proposed modification is provided by the teachings of the '455 reference itself. The cited '455 reference teaches away from the asserted modification by leading in a direction divergent from the path that was taken by Appellant. *In re Haruna*, 249 F.3d 1327, 1335 (Fed. Cir. 2001). The '455 reference

teaches that the first insulating film 16 (*i.e.*, the alleged field plate insulator) is preferably thicker than the second insulating film 18 (*i.e.*, the alleged gate-field plate insulator), while the thickness of film 16 may be determined by a breakdown voltage and the thickness of film 18 may be determined by a threshold voltage. *See, e.g.*, paragraph 0031. The specific example thicknesses given by the '455 reference indicate that film 16 should be substantially thicker than film 18 (*e.g.*, 3,000Å to 30,000Å versus 400Å to 450Å). By expressly teaching that film 16 should be thicker than film 18, the '455 reference teaches a relationship directly opposite, and therefore divergent, from the thickness of the gate-field plate insulator being greater than or equal to the thickness of the field plate insulator, as in the claimed invention. Not only does the '455 reference teach the relationship of the optimal or preferred thicknesses are *opposite* of the Examiner's proposed modification, it teaches that their respective thickness are between *seven to seventy-five times* different (*see, e.g.*, pp. 10:10-11, 25-26).

Modifications are not rendered obvious simply because there is a possibility that one *could* experiment; factual evidence must be sufficient to show that such experimentation would have been obvious. The Examiner provides insufficient factual evidence to support that such a significant modification is suggested to be beneficial or even successful. Moreover, the '455 reference teaches that the thickness is set by "multiplying the static breakdown voltage of the element by 20A" (p. 5:22-26). The Examiner's proposal would therefore appear to suggest a static breakdown voltage of less than 23 volts (*i.e.*, 450/20). This, however, is contrary to one of the main purposes of the '455 reference, which is to realize a high breakdown voltage (*see, e.g.*, p. 5:56-59 and p. 6:5-14; the lowest breakdown voltage shown being twice that of the proposed modification).

Appellant submits that further evidence is provided in the form of Appellant's specification, which includes a clear and persuasive assertion that the source or solution of a problem was not previously recognized. As explained in M.P.E.P. § 2141.02, support for discovery of a problem or solution is evidence of patentability. This evidence can be supported "by way of a clear and persuasive assertion in the specification." Contrary to the M.P.E.P., the Examiner has refused to consider this evidence based upon a mistaken belief that evidence can only be presented "by an appropriate affidavit or declaration" (Advisory

Action, p. 2). Accordingly, this evidence has been improperly excluded from consideration, and this exclusion further supports an inference of improper hindsight reconstruction. This unconsidered evidence includes, but is not limited to the following. "Structures with field plates are known in particular for use with high breakdown voltages of at least 50V and generally higher. The inventors have realized that field plate structures are also applicable to low voltage power MOS-FETs with breakdown voltages of 30V and below, even though the channel resistance forms the major contribution to the resistance in such devices" (p. 3:20-24). Consistent with the teachings of the primary '455 reference, Appellant's specification therefore explains that it was not recognized that devices with low breakdown voltages and corresponding expected high resistances would exhibit successful functionality. Appellant's specification further explains that it was not recognized that an expected punch through effect is absent (p. 3:25-31). The Examiner fails to show or allege any corresponding teachings or suggestions.

For the aforementioned reasons, the factual evidence in favor of the Examiner's position is noticeably absent. The Examiner has primarily relied upon convenient conclusions of experimentation with only vaguely defined goals. The factual evidence in favor of patentability, however, is extensive and supported not only by Appellant's specification, but by the very references presented by the Examiner. Accordingly, the preponderance of evidence supports that the claims are patentable over the cited prior art and the rejections should be reversed.

B. The Rejections of Claims 1-21 are Improper for Lack of Correspondence and Lack of Evidentiary Support Regarding a Doping Concentration that is at Least Fifty Times Greater

The rejections are improper because the cited portions of the '455 reference do not correspond to aspects of the claimed invention directed to the drift region having a steeply graded doping concentration, with the concentration increasing from the body region to the drain region and the concentration being at least 50 times greater adjacent to the drain region than adjacent to the body region. Appellant's disclosure teaches benefits associated with having a steeply graded concentration gradient. *See, e.g.,* Paragraphs 0021-0022. However, the cited portions of the '455 reference provide no appreciation of (or recognition for) such

benefits, and thus, any proposed modification would appear to be improperly based upon Appellant's disclosure. *See, e.g.,* M.P.E.P. § 2142. More specifically, it is not disputed that the cited portions of the '455 reference teach only that the impurity concentration of drift layer 12 increases toward the substrate 11. *See, e.g.,* Figure 2 and Paragraph 0053. The cited portions of the '455 reference do not provide any indication regarding the actual level of impurity concentration in drift layer 12 near well layer 13 relative to the actual level of impurity concentration in drift layer 12 near substrate 11, let alone teach that the doping concentration in the drift region has a steeply graded concentration gradient as in the claimed invention.

The improper nature of the rejection should be apparent due to basis for the rejection being completely independent of the actual doping level. The alleged basis could be applied to any doping level, regardless of the usefulness, suggestiveness or obviousness thereof, showing the insubstantial nature of the argument. The Examiner has not presented any factual evidence that that the doping level was recognized as being a results effective variable with the desired (unidentified) result leading to the claimed doping level. In view of the lack of supporting evidence, the evidence showing the recognition of a benefit by Appellant's specification is more than sufficient. Accordingly, the rejections are improper and should be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-21 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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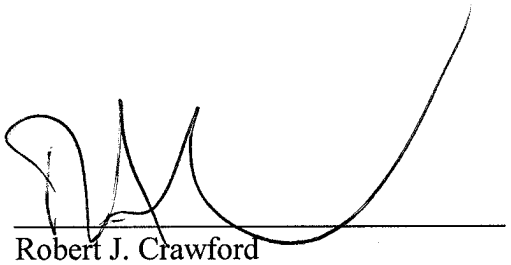
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/580,625)

1. An insulated gate field effect transistor, comprising:

a semiconductor body having opposed first and second major surfaces;

a source region of a first conductivity type at the first major surface;

a body region of a second conductivity type opposite to the first conductivity type under the source region;

a drift region of the first conductivity type under the body region;

a drain region of the first conductivity type under the drift region, so that the source, body, drift and drain regions extend in that order from the first major surface towards the second major surface; and

insulated trenches extending from the first major surface towards the second major surface past the source region and the body region into the drift region, each insulated trench having sidewalls, and including insulator on the sidewalls, at least one conductive gate electrode adjacent to the body region separated from the body region by a gate insulator, and at least one conductive field plate electrode adjacent to the drift region separated from the drift region by a field plate insulator, and a gate-field plate insulator separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being at least as thick as the field plate insulator,

wherein the source regions and the insulated trenches define a pattern of cells across the first major surface; and

a doping concentration in the drift region increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region the doping concentration in the drift region being at least 50 times greater adjacent to the drain region than adjacent to the body region.

2. An insulated gate field effect transistor according to claim 1 in which the conductive gate electrode is of conductive semiconductor doped to be the second conductivity type.

3. An insulated gate field effect transistor according to claim 1 wherein the conductive gate electrode has side pieces spaced apart adjacent to the sidewalls on either side of the insulated trench and a top piece spanning a gap between the side pieces.

4. An insulated gate field effect transistor according to claim 1 wherein a breakdown voltage of the insulated gate field effect transistor is less than or equal to 30V.

5. An insulated gate field effect transistor according to claim 1 wherein the pattern of cells defined by the source regions and the insulated trenches arranged across the first major surface is a pattern in which cells repeat in more than one direction across the first major surface to form a three-dimensional cell structure.

6. An insulated gate field effect transistor according to claim 5 wherein the cells are arranged in a hexagonal pattern.

7. An insulated gate field effect transistor according to claim 1 further comprising an additional trench filled with conductive material extending through the source region to the body region to connect a source contact to the source region and the body region.

8. An insulated gate field effect transistor according to claim 7 further comprising a doped contact region of the second conductivity type in the body region in contact with the conductive material in the additional trench, a doping concentration in the doped contact region being higher than a doping concentration in the rest of the body region.

9. An insulated gate field effect transistor according to claim 1 wherein a thickness of the insulator adjacent to the conductive field plate electrode is greater than a thickness of the insulator adjacent to the conductive gate electrode.

10. An insulated gate field effect transistor according to claim 1 wherein the pattern of cells has a cell pitch not greater than 1 micron.

11. An insulated gate field effect transistor according to claim 1 wherein the first conductivity type is n-type, the second conductivity type is p-type and the conductive gate electrode is of p-type doped polysilicon.

12. An insulated gate field effect transistor according to claim 1 wherein the field plate insulator has a thickness between 0.6 to 1 microns and the gate insulator has a thickness between 0.2 to 0.5 microns.

13. An insulated gate field effect transistor according to claim 1 wherein the conductive field plate electrode is connected to the source region.

14. An insulated gate field effect transistor according to claim 1 further comprising

a field plate terminal connected to the conductive field plate electrode for controlling a field plate voltage independently.

15. An insulated gate field effect transistor, comprising:

a semiconductor body having opposed first and second major surfaces;

a source region of a first conductivity type at the first major surface;

a body region of a second conductivity type opposite to the first conductivity type under the source region;

a drift region of the first conductivity type under the body region;

a drain region of the first conductivity type under the drift region, so that the source, body, drift and drain regions extend in that order from the first major surface towards the second major surface; and

insulated trenches extending from the first major surface towards the second major surface past the source region and the body region into the drift region, each insulated trench having sidewalls, and including insulator on the sidewalls, at least one conductive gate electrode adjacent to the body region separated from the body region by a gate insulator, and at least one conductive field plate electrode adjacent to the drift region separated from the

drift region by a field plate insulator, and a gate-field plate insulator separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being thicker than the field plate insulator,

wherein the source regions and the insulated trenches define a pattern of cells across the first major surface; and

wherein the drift region has a graded doping concentration that increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region, the doping concentration in the part of the drift region adjacent to the drain region being at least 50 times greater than the doping concentration in the part of the drift region adjacent to the body region.

16. An insulated gate field effect transistor according to claim 15, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 200 times greater than the doping concentration in the part of the drift region adjacent to the body region.

17. An insulated gate field effect transistor according to claim 15, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 100 times greater than the doping concentration in the part of the drift region adjacent to the body region.

18. An insulated gate field effect transistor according to claim 15, further comprising a source contact and an additional trench filled with conductive material, the additional trench extending through the source region to the body region, the conductive material in the additional trench connecting the source contact to the source region and to the body region.

19. An insulated gate field effect transistor, comprising:

a semiconductor body having opposed first and second major surfaces;

a source region at the first major surface, a body region under the source region, a drift region under the body region, and a drain region under the drift region, the drift region having a doping concentration that increases from a part of the drift region adjacent to the body region to a part of the drift region adjacent to the drain region, the doping concentration in the drift region being at least 50 times greater adjacent to the drain region than adjacent to the body region; and

a plurality of insulated trenches extending from the first major surface into the drift region, each of the insulated trenches including

at least one conductive gate electrode adjacent to the body region and separated from the body region by a gate insulator,

at least one conductive field plate electrode adjacent to the drift region and separated from the drift region by a field plate insulator, and

a gate-field plate insulator separating the conductive field plate electrode from the conductive gate electrode, the gate-field plate insulator being at least as thick as the field plate insulator,

wherein the source regions and the insulated trenches define a pattern of cells across the first major surface.

20. An insulated gate field effect transistor according to claim 19, wherein the conductive gate electrode in each of the insulated trenches includes

two vertical side pieces spaced apart from each other and adjacent to sidewalls on either side of the insulated trench, and

a horizontal top piece spanning a gap between and connecting the two side pieces.

21. An insulated gate field effect transistor according to claim 15, wherein the drift region has a steeply graded doping concentration that is defined by the ratio of the doping concentration of the part of the drift region adjacent to the drain region to the doping

concentration of the part of the drift region adjacent to the body region and wherein the ratio is greater than at least one of: 50, 100 or 200.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.